REMARKS

The Final Office Action mailed on August 14, 2002, has been received and reviewed. Claims 1-17 are currently pending in the above-referenced application. Each of claims 1-17 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1, 2, 8, 9, 11, 16, and 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,278,153 to Kikuchi et al. (hereinafter "Kikuchi").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

It is respectfully submitted that claim 1, as proposed to be amended, and claims 2, 8, 9, 11, 16 and 17 which depend from claim 1, are not anticipated by Kikuchi because Kikuchi fails to expressly or inherently describe every element recited in these claims. In particular, Kikuchi fails to expressly or inherently describe teach a method for disposing a material on a semiconductor device structure over at least one recess, in which method the material is disposed in such a way that at least the portion of the material located over or within the at least one recess has a substantially planar upper surface.

Kikuchi shows, in Fig. 6D, an intermediate semiconductor device structure in which a layer of resist 20 that has been disposed within and over a via-hole 23a appears to have a planar surface. Kikuchi also discloses that the resist 20 can be applied by several methods known in the art, including spin-coating. Col. 17, lines 63-66. However, as pointed out by the "Background" section of the specification of the above-referenced application, at page 3, line 15, to page 4, line 29, the limitations in previously known spin-on methods, as well as material properties (*e.g.*,

surface tension, adherence to adjacent materials, etc.), prevent a layer of material, such as the resist 20 disclosed by Kikuchi and illustrated in Fig. 6D, from having a substantially planar upper surface. As such, it is respectfully submitted that Kikuchi neither expressly nor inherently describes that resist 20 is disposed on a surface of a semiconductor device structure 21 such that the resist 20 over or within a via-hole 23a thereof has an upper surface which is substantially planar.

Therefore, claim 1, as proposed to be amended, is not anticipated by Kikuchi. Thus, amended claim 1 is allowable under 35 U.S.C. § 102(e).

Claims 2, 8, 9, 11, 16, and 17 are each further allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 2, which is rejected as being anticipated by Figs 6A-6D; 10A-10E; 13A-13E, is further allowable since none of these figures shows disposing a material "so as to substantially fill . . . at least one recess *without substantially covering* [a] surface of a semiconductor device structure . . ." While various figures that have been referenced, including Figs. 6E, 10D, 10E, and 13E, show structures which include recess that are substantially filled with material while the same material does not cover the surfaces of the illustrated semiconductor devices, conventional techniques are used to form these structures. As is well known and described in Kikuchi, such conventional techniques disposing an excessive quantity of material onto the surface of a semiconductor device structure to fill the recesses, which results in the surface of the semiconductor device structure also being covered with the material. Excess material is then removed from the surface of the semiconductor device structure in such a way as to leave the recesses filled. The "disposing" of Kikuchi, therefore, is not effected "without substantially covering said surface."

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, 8, 9, 11, 16, and 17 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Kikuchi in View of Yoshihara

Claims 3-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara").

It is respectfully submitted that claims 3-7 are allowable, among other reasons, as depending either directly or indirectly from claim 1, which is itself allowable.

Moreover, neither Kikuchi, Yoshihara, nor knowledge available to one ordinarily skilled in the art suggests the combination of the teachings of Kikuchi with Yoshihara to arrive at invention which is recited in claims 3-7. Kikuchi teaches that layers of resist may be spin-coated onto semiconductor substrates that include recesses. However, Kikuchi neither teaches or suggests that resist layers so formed have substantially planar surfaces, at least over or within the recesses of such semiconductor substrates. Yoshihara teaches that by spinning a semiconductor wafer at high speeds ("as low as 2000 rpm" Col. 11, line 16), lowering the speed for a time, and re-increasing it to high speeds, the wafer can be coated with material in such a way that circular ripples do not appear thereon. Yoshihara does not, however, suggest that the techniques described therein are useful for disposing material within recesses such that the upper surface of at least the material within or over the recesses has a substantially planar upper surface. Accordingly, it is respectfully submitted that one of ordinary skill in the art would not have been

motivated to combine the teachings of Kikuchi and Yoshihara in the manner that has been asserted.

Moreover, it appears that any motivation to combine the teachings of Kikuchi and Yoshihara could only have been improperly gleaned from the benefit of hindsight provided by the disclosure of the above-referenced application.

For the above reason, the ordinarily skilled artisan would also likely consider the likelihood of success when combining Kikuchi and Yoshihara to be quite low.

Finally, the combination does not teach or suggest each and every element of claim 5. In particular, neither Kikuchi nor Yoshihara teaches or suggests initially spinning a semiconductor device structure at a rate of about 1,000 rpm, as recited in claim 5. Instead, the initial spin rate taught by Yoshihara is "as low as 2000 rpm . . ." col. 11, line 16.

Kikuchi in View of Lin

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,046,083 to Lin et al. (hereinafter "Lin").

It is respectfully submitted that claim 10 is allowable, among other reasons, as depending upon claim 1, which is itself allowable and, thus, the arguments pertaining to claim 1 apply.

Kikuchi in View of Park

Claims 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kikuchi in view of U.S. Patent 6,326,282 to Park et al. (hereinafter "Park").

It is respectfully submitted that claims 12-15 are allowable, among other reasons, as depending either directly or indirectly upon claim1, which is itself allowable and, thus, the arguments pertaining to claim 1 apply.

Furthermore, the combination of references does not teach or suggest each and every element of either claim 14 or claim 15.

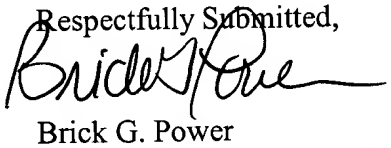
ENTRY OF AMENDMENTS

It is respectfully submitted that the amendments proposed herein should be entered since they are supported by the as-filed specification, do not introduce new matter into the above-referenced application, do not raise new issues, and would not require an additional search. Moreover, it is respectfully submitted that, by placing the claims in condition for allowance, the proposed amendments narrow the issues that would be present on appeal. Finally, if the proposed amendments are not entered, entry thereof upon filing of a Notice of Appeal in the above-referenced application is respectfully requested.

CONCLUSION

It is respectfully submitted that claims 1-17 are allowable. An early notice of the allowability of these claims and an indication that the above-referenced application has been passed for issuance are respectfully solicited. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully Submitted,



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Enclosure: Version of Claims with Markings to Show Changes Made

BGP/hlg:djp
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VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Twice amended) A method for disposing a material on a semiconductor device structure, comprising:

providing a semiconductor device structure including a surface and at least one recess formed in said surface;

disposing said material on said surface so as to substantially fill said at least one recess, said material covering said surface having a thickness less than a depth of said at least one recess without subsequently removing said material from [over] said surface, an upper surface of at least a portion of said material over or within said at least one recess being substantially planar.